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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,124	08/08/2000	Norio Fukasawa	980233A	4720

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,124	FUKASAWA ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a) In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7-10,12,21,22,24-29,32-35,40,65-69,78,86 and 88-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12,27-29 and 65-69* is/are allowed.

6)☒ Claim(s) *1,4,5,7-10,21,22,24-26,32-35,40,78,86 and 88-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The amendment to the claims filed 11-27-2 is non-responsive to the last Office action because it fails to conform to the provisions of MPEP 714.03:

> 714.03 Amendments Not Fully Responsive - Action To Be Taken: Where a bona fide response to an examiner's action is filed before the expiration of a permissible period, but through an apparent oversight or inadvertence some point necessary to a complete response has been omitted - such as an amendment or argument as to one or two of several claims involved or signature to the amendment - the examiner, as soon as he or she notes the omission, should require the applicant to complete his or her response within a specified time limit (usually one month) if the period for response has already expired or insufficient time is left to take action before the expiration of the period. If this is done the application should not be held abandoned even though the prescribed period has expired.

Specifically, the 35 U.S.C. 103(a) rejection of claim 26 has not been addressed.

Because the response appears to be bona fide, but through an apparent oversight or inadvertence the response is incomplete, and in order to continue to afford applicant the benefit of compact prosecution, the requirement to complete the response within a one month time limit is waived, the amendment is entered, and the claims are examined on the merits.

Claim 40 is rejected as incomplete because it depends on canceled claim 37. See MPEP 608.01(n)V.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Lim (5925934).

At column 6, line 61 to column 9, line 8, and column 10, lines 4-14, Lim teaches the following:

1. A method for fabricating a semiconductor device comprising: a resin sealing step of loading a substrate 570 on which semiconductor elements having protruding electrodes 520 are formed to a mold 615, and supplying a sealing resin 545 to positions of the protruding electrodes so as to form a resin layer which seals the protruding electrodes and the substrate; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated from each other, wherein the resin sealing step disposes a film 570 between the protruding electrodes and the mold [top mold half] which thus contacts the sealing resin through the film.

35. The method for fabricating the semiconductor device as in 1, wherein the sealing resin is processed in positions in which positioning protruding electrodes 520 are formed in order to discriminate the protruding electrodes and the positioning protruding electrodes from each other.

To further clarify the teaching of a separating step of cutting the substrate together with the resin layer, as cited, Lim teaches "excising" the substrate, portions of which remain encapsulated together with the resin layer.

To further clarify the teaching wherein the sealing resin is processed in positions in which positioning protruding electrodes are formed in order to discriminate the protruding electrodes and the positioning protruding electrodes from each other, it is noted that the resin is processed in order to distinguish each of the electrodes from each other by exposing differences in locations of the electrodes.

To further clarify the teaching that the mold contacts the sealing resin through the film, the mold, at least physically, thermally and electrically, contacts the resin through the film portion that is clamped between the molds, extends through the resin, and is attached to the chip at 530.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered

therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim as applied to claims 1 and 35, and further in combination with Ohta (5641997).

Lim does not appear to explicitly teach the following: 4. The method for fabricating the semiconductor device as in 1 wherein: the mold used in the resin sealing step comprises an upper mold which can be elevated, and a lower mold having a first lower mold half body which is kept stationary and a second lower mold half body which can be elevated with respect to the first lower mold half body; and the resin sealing step comprises: a substrate loading step of placing the substrate on which the semiconductor elements having the protruding electrodes are arranged in a cavity defined by a cooperation of the first and second lower mold half bodies and providing the sealing resin the cavity; a resin layer forming step of moving down the upper mold and the second lower mold half body so that

the sealing resin is heated, melted and compressed so that the resin layer sealing the protruding electrodes is formed; and a detaching step of moving up the first mold so as to detach the upper mold from the resin layer, and then moving down the second lower mold half body from the first lower mold half body so that the substrate to which the resin layer is provided is detached from the mold.

88. A method for fabricating the semiconductor as in 4, wherein the resin sealing step further comprises a film disposing step of providing a non-adhesive process film between contact surfaces of the upper mold and the first lower mold half body and the second lower mold half body.

Nonetheless, at column 6, lines 32-65, column 7, lines 13-19, column 9, lines 23-34, column 11, lines 15-63, and column 54, lines 56-64, Ohta teaches wherein a mold used in a resin sealing step comprises an upper mold 9a which can be elevated, and a lower mold having a first lower mold half body 8b which is kept stationary [after clamping] and a second lower mold half body 9b which can be elevated with respect to the first lower mold half body; and a resin sealing step comprises: a substrate loading step of placing a substrate 3 on which a semiconductor element 5 having protruding electrodes 4 is arranged in a cavity defined by a cooperation of the first and second lower mold half

bodies and providing the sealing resin 1 in the cavity; a resin layer forming step of moving down the upper mold and moving the second lower mold half body so that the sealing resin is heated, melted and compressed so that the resin layer sealing the protruding electrodes is formed, a detaching step of moving the mold so as to detach the upper mold from the resin layer, and so that the substrate to which the resin layer is provided is detached from the mold, wherein the resin sealing step further comprises a film disposing step of providing a non-adhesive process film ["releasing agent"] between contact surfaces of the upper mold and the first lower mold half body and the second mold half body. Additionally, it would have been obvious to combine the process of Ohta with the process of Lim because it would facilitate resin sealing.

Although the applied prior art does not appear to explicitly teach the entire particular mold moving sequence, as cited, Ohta teaches that the upper mold half and the second lower mold half body are movable up and down, and it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed mold moving sequence because applicant has not disclosed that the sequence is for a particular unobvious purpose,

produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim as applied to claims 1 and 35, and further in combination with Ohta (5641997).

Lim does not appear to explicitly teach the following: 5. The method for fabricating the semiconductor device as in 1, wherein: an excess resin removing mechanism is provided in the mold used in the resin sealing step; and the excess resin removing mechanism removes excess resin and controls a pressure applied to the sealing resin in the mold. Notwithstanding, as cited supra, Ohta teaches this process. Moreover, it would have been obvious to combine the process of Ohta with the process of Lim because it would facilitate resin sealing.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim as applied to claims 1 and 35, and further in combination with Ota (JP5343458).

Lim does not appear to explicitly teach the following:

7. The method for fabricating the semiconductor device as in 1, wherein the sealing resin is provided to the film before the resin sealing step is executed.

8. The method for fabricating the semiconductor device as in 7, wherein a plurality of sealing resins are provided to the film, and the resin sealing step is continuously carried out by moving of the film.

Nevertheless, in the English abstracts and figures, Ota teaches wherein a sealing resin 2 is provided to a film 7 before a resin sealing step is executed, a plurality of sealing resins 1, 2 are provided to the film, and the resin sealing step is continuously carried out by moving of the film. In addition, it would have been obvious to combine the process of Ota with the process of Lim because it would facilitate resin sealing.

Claims 1, 24, 25 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kihira (JP864725) and Tanaka (JP63308329).

In the English abstract, translation and figures, Kihira teaches the following:

1. A method for fabricating a semiconductor device comprising: a resin sealing step of loading a substrate 11 on which semiconductor elements having protruding electrodes 16 are formed to a mold 21a, 21b, and supplying a sealing resin 19 to

positions of the protruding electrodes so as to form a resin layer which seals the protruding electrodes and the substrate; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated from each other.

However, Kihira does not appear to explicitly teach wherein the resin sealing step disposes a film between the protruding electrodes and the mold which thus contacts the sealing resin through the film, and the following:

24. The method for fabricating the semiconductor device as in 1, wherein: the film used in the resin sealing step has projections located in positions corresponding to those of the protruding electrodes; and the resin layer is formed in a state in which the projections are pressed against the protruding electrodes.

34. The method for fabricating the semiconductor device as in 1, wherein: the film used in the resin sealing step has projection or recess portions located in positions in which the film is not interfered with the projecting electrodes; and recess or projection portions formed on the resin layer by the projection or recess portions are used for positioning after the resin sealing step is completed.

Nonetheless, in the English abstracts and figures, Tanaka teaches wherein a resin sealing step disposes a film 17 between protruding electrodes 12 and a mold 14, 15 which thus contacts the sealing resin 18 through the film, the film used in the resin sealing step has projections located in positions corresponding to those of the protruding electrodes, the resin layer is formed in a state in which the projections are pressed against the protruding electrodes, the film used in the resin sealing step has projection portions located in positions in which the film is not interfered with the projecting electrodes, and recess portions formed on the resin layer by the projection portions are used for positioning after the resin sealing step is completed. Moreover, it would have been obvious to combine the process of Tanaka with the process of Kihira because it would enable exposure of the electrodes while simplifying mold construction.

To further clarify the teaching that the recess portions formed on the resin layer by the projection portions are used for positioning after the resin sealing step is completed, it is noted that the purpose of the recess portions of Tanaka is to expose the electrodes for electrical connection, and it is inherent in the process of electrode connection that they are used for positioning.

In addition, in the combination of Kihira and Tanaka, Kihira teaches the following:

25. The method for fabricating the semiconductor device as in 1, wherein: an external connection protruding electrode forming step is executed which forms external connection protruding electrodes 20 on the ends of the protruding electrodes after the ends of the protruding electrodes are exposed from the resin layer in the protruding electrode exposing step.

Claims 9, 10, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kihira and Tanaka as applied to claims 1, 24, 25 and 34, and further in combination with Lerner (5381042).

Kihira and Tanaka do not appear to explicitly teach the following:

9. The method for fabricating the semiconductor device as in 1, wherein, a reinforcement plate is loaded onto the mold before the substrate is loaded onto the mold in the resin sealing step.

10. The method for fabricating the semiconductor device as in 9, wherein the reinforcement plate comprises a substance having a heat radiating performance.

21. The method for fabricating the semiconductor device as in 9, further comprising a reinforcement plate to which the sealing resin is provided beforehand in the resin sealing step.

22. The method for fabricating the semiconductor device as in 21, wherein: a frame extending towards the substrate in a state in which the reinforcement plate is loaded onto the mold is formed to define a recess portion; and the resin layer is formed on the substrate by using, as a cavity for resin sealing, the recess portion in the resin sealing step.

Nonetheless, at column 4, line 29 to column 5, line 64, Lerner teaches wherein, a reinforcement plate 400 is loaded onto a mold 500 before a substrate 521 is loaded onto the mold in a resin sealing step, the reinforcement plate comprises a substance having a heat radiating performance, a reinforcement plate to which the sealing resin 601 is provided beforehand [before the package 600 is removed] in the resin sealing step, and a frame 400 extending towards the substrate in a state in which the reinforcement plate is loaded onto the mold is formed to define a recess portion 510, and the resin layer is formed on the substrate by using, as a cavity for resin sealing, the recess portion in the resin sealing step. In addition, it would have been obvious to combine the process of Lerner with the process of Kihira and Tanaka because it would improve heat dissipation.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kihira and Tanaka as

applied to claims 1, 24, 25 and 34, and further in combination with Lynch (5698465).

Kihira and Tanaka does not appear to explicitly teach the following:

26. The method for fabricating the semiconductor device as in 25, wherein the protruding electrodes and the external connection protruding electrodes are bonded by using a bonding member having a characteristic of stress relaxation in the external connection protruding electrode forming step.

Notwithstanding, at column 4, lines 60-65, Lynch teaches wherein a protruding electrode 26 and an external connection protruding electrode 36 are bonded by using a bonding member 36 having a characteristic of stress relaxation in an external connection protruding electrode forming step. Moreover, it would have been obvious to combine the process of Lynch with the process of the applied prior art because it would provide an external connection protruding electrode.

Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim as applied to claims 1 and 35, and further in combination with Romano (4887149).

Lim does not appear to explicitly teach the following:

32. The method for fabricating the semiconductor device as in 1, wherein positioning grooves are formed on a back surface of the

resin layer of the substrate after the resin sealing step is executed and before the separating step is executed.

33. The method for fabricating the semiconductor device as in 32 characterized in that the positioning grooves are formed by subjecting the back surface to half scribing.

Nevertheless, at column 3, line 65 to column 5, line 54, Romano teaches wherein positioning grooves 7, 7', 8, 8' are formed on a back surface of a resin layer 5, 6 of a substrate 13 after a resin sealing step is executed, characterized in that the positioning grooves are formed by subjecting the back surface to half scribing. In addition, it would have been obvious to combine the process of Romano with the process of Lim because it would facilitate positioning of the semiconductor device on a heat sink.

Although the applied prior art does not appear to explicitly teach that the positioning grooves are formed before the separating step is executed, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the sequence is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that,

in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Claim 89 is rejected under 35 U.S.C. 102(a) as being anticipated by Kihira (JP864725).

As cited supra, Kihira teaches the following:
89. A method for fabricating a semiconductor device, comprising the steps of: an encapsulating step of supplying a rigid sealing material 19 to a substrate on which protruding electrodes are formed so as to form an encapsulation layer which seals the protruding electrodes and the substrate; a stiffening step of heating the encapsulation layer; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated from each other.

To further clarify the teaching of an encapsulating step of supplying a rigid sealing material 19, it is noted that some degree of rigidity is an inherent property of the sealing material both in the uncured and cured state.

Claim 86 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamaji (5394303).

At column 2, line 51 to column 4, line 34, Yamaji teaches the following:

86. A method for fabricating a semiconductor device, comprising: a semiconductor device main body forming step of forming a semiconductor device main body 1 having a semiconductor element having a surface on which protruding electrodes 2_1, 2_2 are directly formed, and a layer 4 which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; an interposer forming step of forming an interposer 3 to which the semiconductor device main body is attached, a wiring pattern 7_1 to which the semiconductor device main body is connected being formed on a base member of the interposer; a conductive member arranging step of arranging a conductive member 5_1 to at least one of the semiconductor device main body and the interposer; a bonding step of bonding the semiconductor device main body and the interposer by an adhesive 4 and connecting them electrically; and an external connection terminal forming step of forming external connection terminals 6_3, 6_4 which are connected to the wiring pattern through holes 8 formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided.

Claim 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji as applied to claim 86, and further in combination with Pennisi (5136365)

As cited supra, Yamaji teaches the following:

78. A method for fabricating a semiconductor device, comprising: a semiconductor device main body forming step of forming a semiconductor device main body having a semiconductor element having a surface on which protruding electrodes are directly formed, and a layer which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; an interposer forming step of forming an interposer to which the semiconductor device main body is attached, a wiring pattern to which the semiconductor device main body is connected being formed on a base member of the interposer; a bonding step of bonding the semiconductor device main body and the interposer by a conductive film [solder] which has an adhesiveness and a conductivity in a pressed direction, the conductive film fixing the semiconductor device main body to the interposer and electrically connecting them; and an external connection terminal forming step of forming external connection terminals which are connected to the wiring pattern through holes formed in the base member and are arranged on a surface of

the semiconductor device main body opposite to the surface on which the protruding electrodes are provided.

However, Yamaji does not appear to explicitly teach that the conductive film is an anisotropic conductive film.

Regardless, at column 3, line 54 to column 4, line 15, and column 5, lines 18-23, Pennisi teaches a bonding step of bonding an integrated circuit device main body 230 and a substrate 200 by an anisotropic conductive film 220 which has an adhesiveness and a conductivity in a pressed direction, the conductive film fixing the integrated circuit device main body to the substrate and electrically connecting them. Furthermore, it would have been obvious to combine the process of Pennisi with the process of Yamaji because it would facilitate electrical connection.

Claim 90 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ota (JP5343458), Kihira (JP864725) and Tanaka (JP63308329).

As cited supra, Ota teaches the following:

90. A method for fabricating a semiconductor device comprising: a mold preparing step of preparing a mold including a first mold 9a, and a second mold which is located so as to face the first mold, the second mold including a first half body 9b having a shape corresponding to a shape of a substrate, and a second half body 8b which is provided so as to surround the first half body

and can be elevated with respect to the first half body, the first and second half bodies cooperating with each other so that a cavity to be filled with resin is defined; a resin sealing step of placing the substrate 5 on which a semiconductor element equipped with protruding electrodes 4 is formed in the mold and supplying resin 1 to positions in which the protruding electrodes are provided so as to form a resin layer which seals the protruding electrodes and the substrate.

However, Ota does not appear to explicitly teach a plurality of semiconductor elements, a protruding electrode exposing step of exposing at least end portions of the protruding electrodes from the resin layer, and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated into each other.

Notwithstanding, as cited supra, Kihira teaches this process. In addition, it would have been obvious to combine the process of Kihira with the process of Ota because, as taught by Kihira, it would enable highly integrated packaging.

Also, Ota does not appear to explicitly teach wherein the resin sealing step disposes a film, between the protruding electrodes and the mold, which thus contacts the sealing resin through the film.

Regardless, as cited supra, Tanaka teaches this limitation. Furthermore, it would have been obvious to combine the process of Tanaka with the process of Ota and Kihira because it would enable exposure of the electrodes while simplifying mold construction.

Applicant contends that Tanaka does not teach a film.

This contention is respectfully traversed because Tanaka teaches a thin covering or coating 17, therefore, Tanaka teaches a film 17.

Also, applicant alleges that the combination of Tanaka and Kihira would be inoperable. However, applicant provides no factual support for this allegation. Hence, the allegation is respectfully deemed unpersuasive because it is of no probative value. See MPEP 716.01(c).

In addition, applicant asserts that Kihira does not teach a rigid sealing material, and further defines the term *rigid sealing material* to be "a sealing resin containing a large amount of fillers."

This assertion is respectfully traversed because the scope of the term *rigid sealing material* is not limited to "a sealing resin containing a large amount of fillers." Furthermore, Kihira is not necessarily applied to the rejection for a teaching of a sealing resin containing a large amount of fillers.

Relatedly, applicant argues that Kihira does not teach that the sealing material 19 is "rigid when it is supplied in its encapsulating step."

This argument is respectfully traversed because Kihira is explicitly and clearly applied to the rejection for a teaching of "an encapsulating step of supplying a rigid sealing material 19." To further clarify, the sealing material, both in the cured and uncured state, is provided by an encapsulating step; therefore, it is supplied by an encapsulating step.

Also, applicant contends that Yamaji does not teach a layer which is formed on the surface of the semiconductor element.

This contention is respectfully traversed because as explicitly and clearly recited in the rejection, Yamaji teaches a layer 4 which is formed on the surface of the element. To further clarify, it is noted that the layer is formed on the surface of the element either after being formed on the film 3, or as cited in the rejection, at column 3, lines 58-59, before being formed on the film.

Claims 12, 27-29 and 65-69 are allowed.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/308-7722.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
31-May-03